NEC 304

STLD

Lecture 38

Programmable Logic

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Overview

° **Programmable logic offers designers opportunity to *customize* chips**

° **Programmable logic devices have a fixed logic structure**

° **Programmable array logic contain AND-OR circuits**

- **First introduced in early 1980's**

° **Field programmable gate arrays (FPGAs) contain small blocks that implement truth tables**

- **First introduced in 1985 (Xilinx Corporation)**

° **Software used to convert user designs to programming information**

Design Implementation

- **Chip creation is a long and difficult process**
- **Millions of dollars required to create custom silicon**
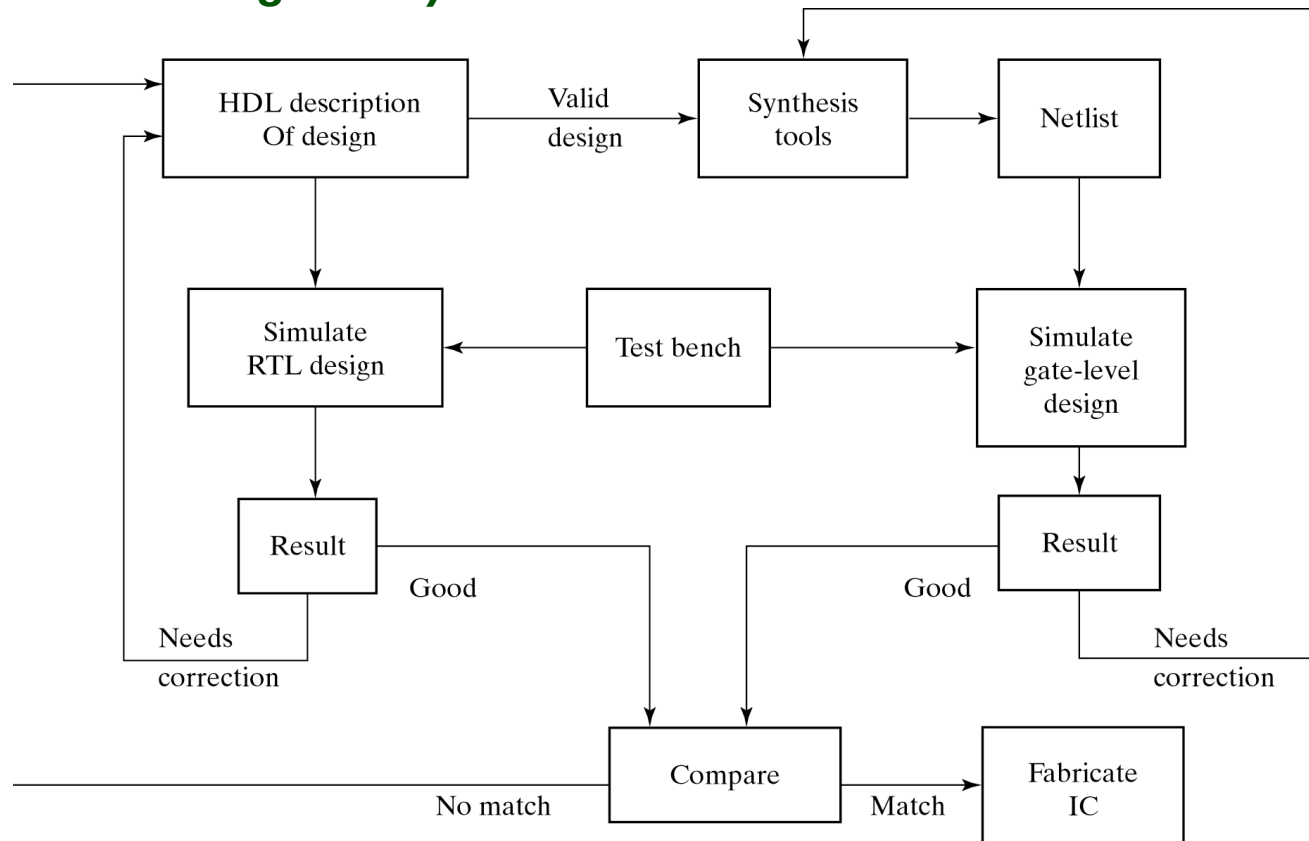 - **Simulation, synthesis, fabrication (lots of jobs for engineers)**

Fig. 8-1 Process of HDL Simulation and Synthesis

Programmable Logic Design

° **"Generic" chip created and then customized by designer**

° **Programming information used**

- **Like a ROM**

° **Analogy – sign making**

- **Custom sign – more expensive, customized by manufacturer, difficult to change**

- **Sign built by consumer from individual letters – less expensive, not quite as nice, easier to change (remix letters)**

ENGIN112

R

N

Z

V

M

E N G I N 1 1 2

Programmable Array Logic

- **Implements sum-of-products expressions**

- **Four external inputs (and complements)**

- **Feedback path from output F_1**

- **Product term connections made via switches**
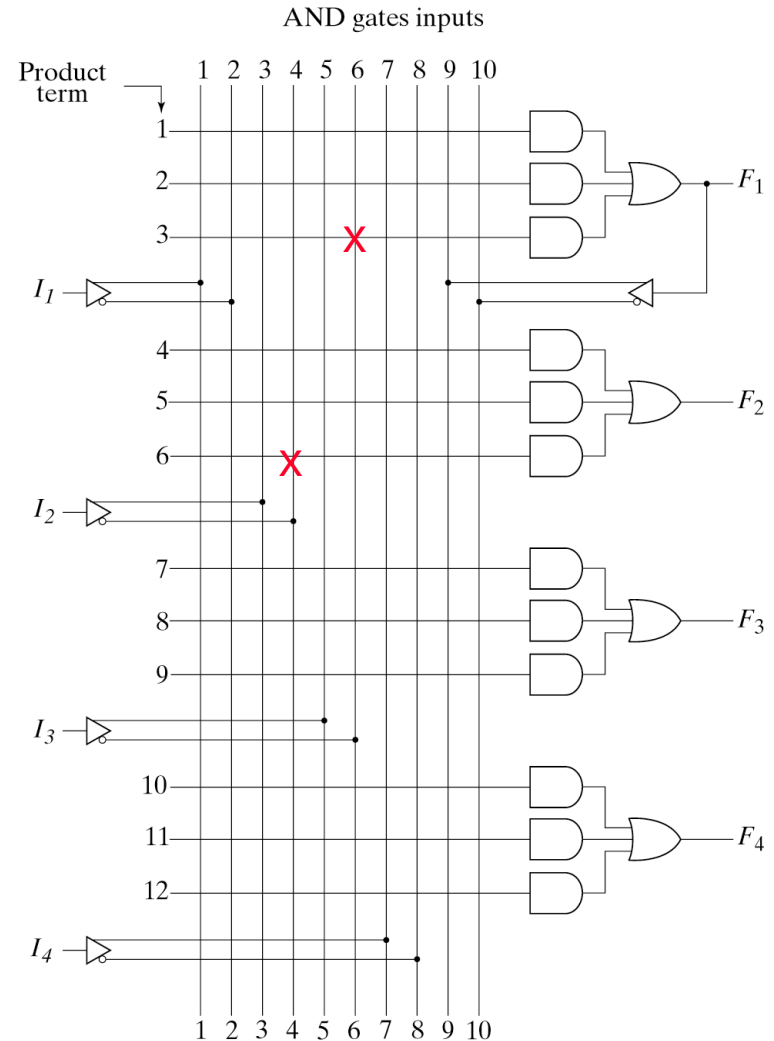
AND gates inputs

Fig. 7-16 PAL with Four Inputs, Four Outputs, and Three-Wide AND-OR Structure

Programmable Array Logic

- **Consider implementing the following expression**

  - $I_1 I_2 I_3 + I_2' I_3' I_4 + I_1 I_4 = F_1$

- **Note that only functions of up to three product terms can be implements**

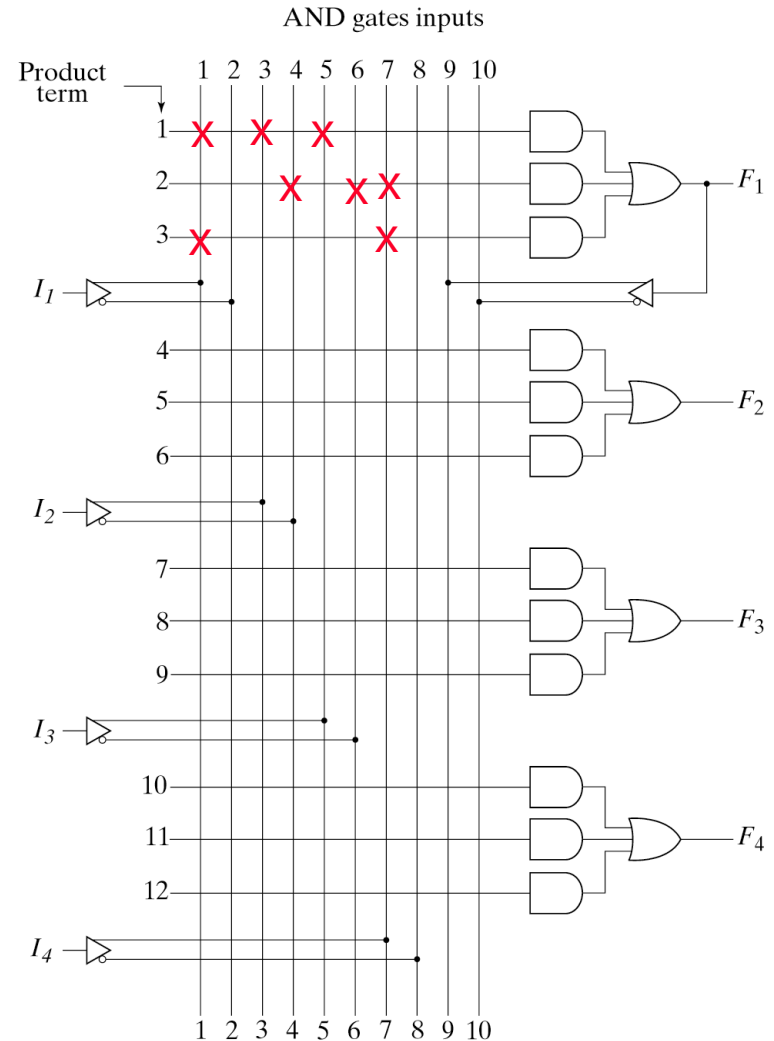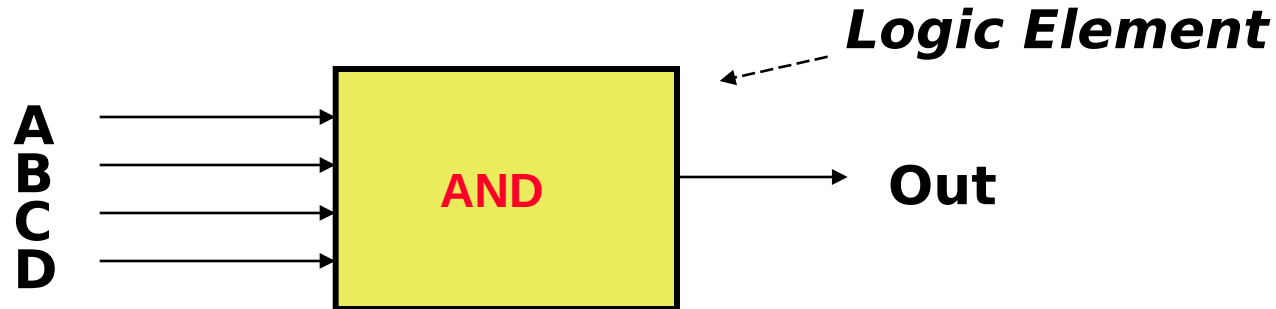 - **Larger functions need to be chained together via the feedback path**

AND gates inputs

Product term

1 2 3 4 5 6 7 8 9 10

F_1

I_1

F_2

I_2

F_3

I_3

F_4

I_4

1 2 3 4 5 6 7 8 9 10

Fig. 7-16 PAL with Four Inputs, Four Outputs, and Three-Wide AND-OR Structure

Reconfigurable Hardware

Logic Element

A
B   AND   Out
C
D

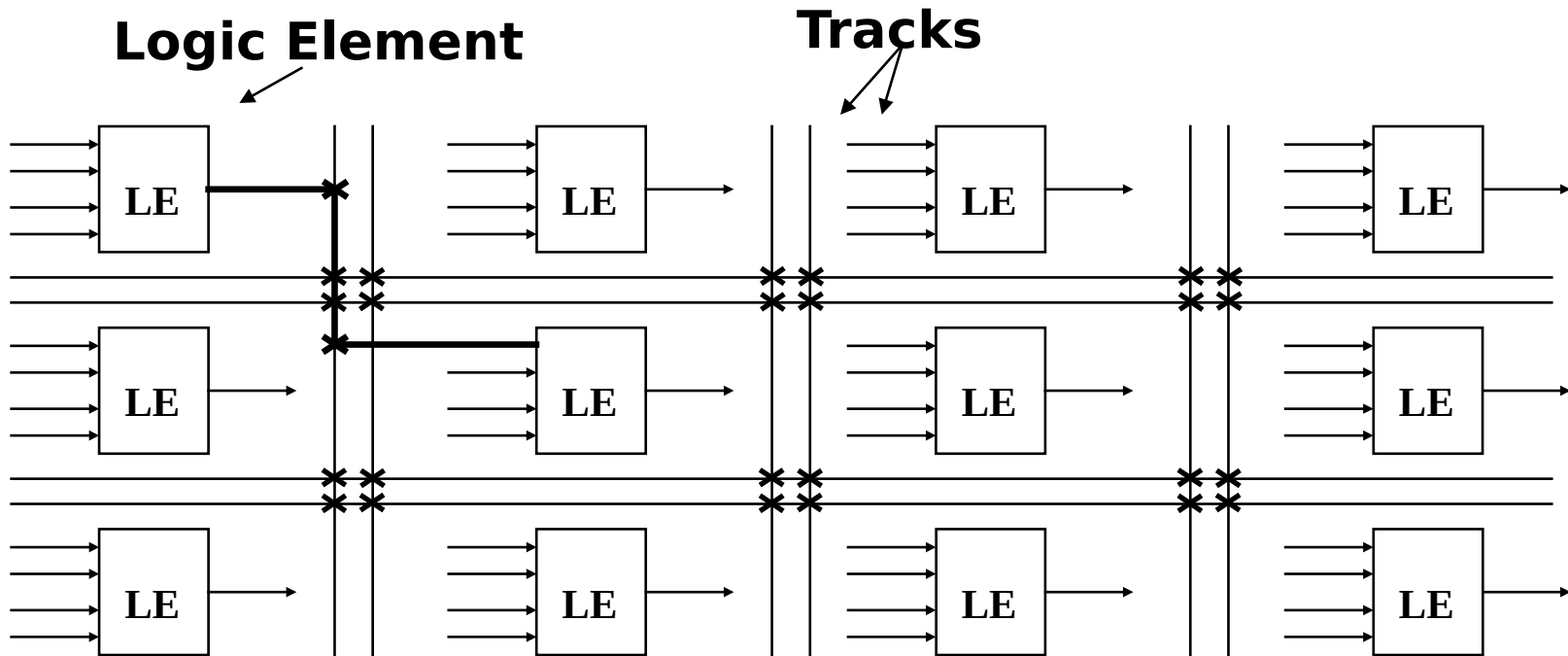## A . B . C . D = out

- **Each logic element operates on four one-bit inputs.**

- **Output is one data bit.**
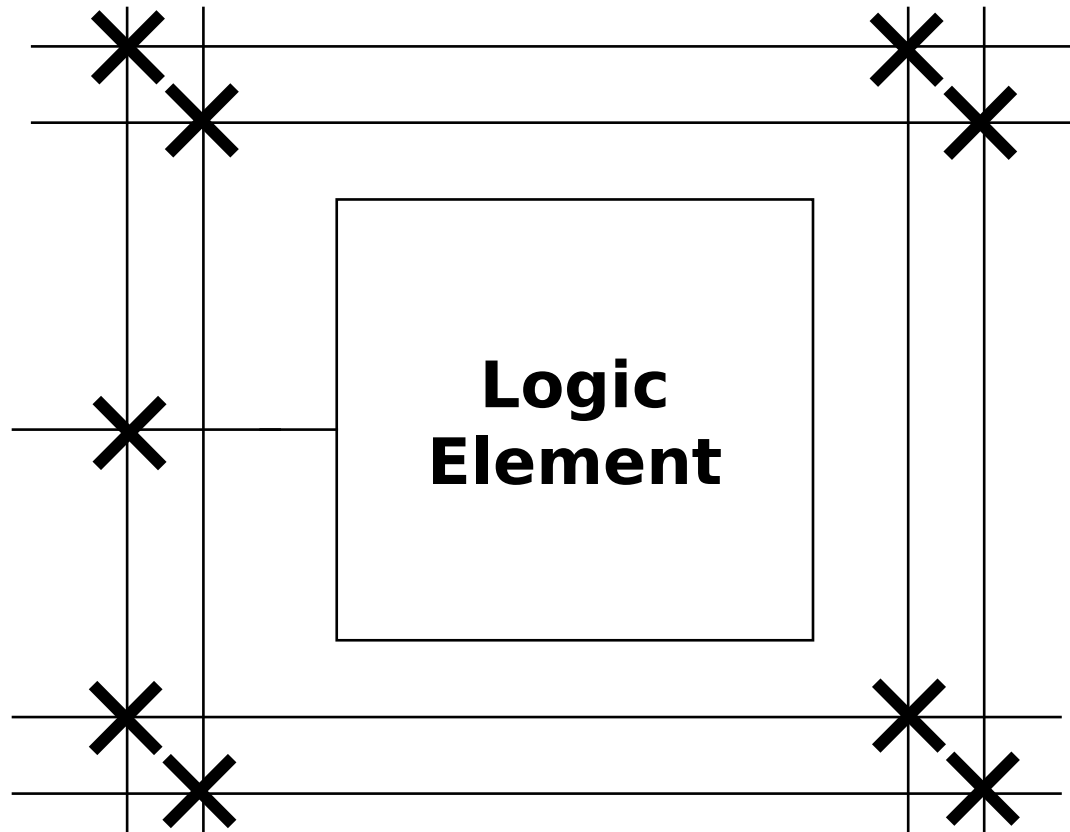
- **Can perform <u>any</u> Boolean function of four inputs**

2^{2^4} **= 64K functions!**

Field-Programmable Gate Array

Logic Element

Tracks

- **Each *logic element* outputs one data bit.**
- **Interconnect programmable between elements.**
- **Interconnect *tracks* grouped into channels.**
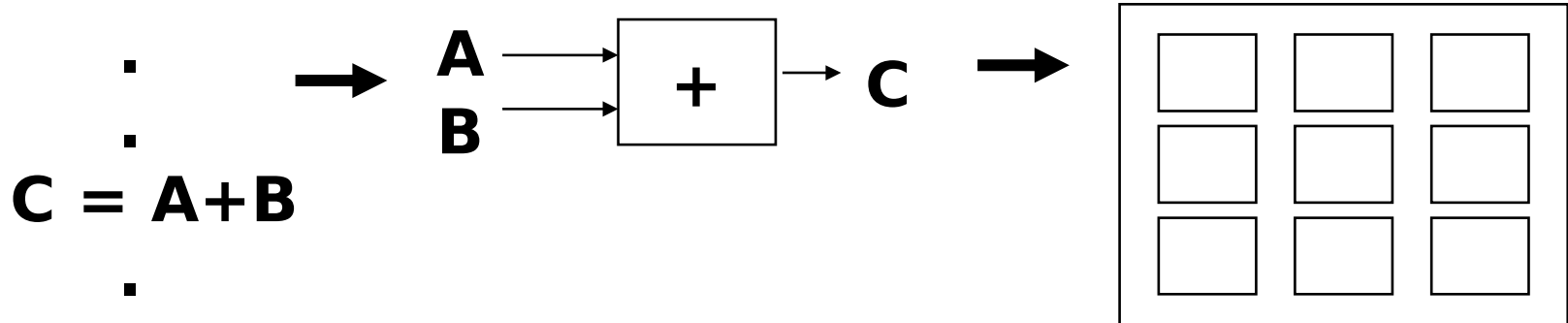
FPGA Architecture Issues

Logic Element

- **Need to explore architectural issues.**
- **How much functionality should go in a logic element?**
- **How many routing tracks per channel?**
- **Switch "population"?**

Translating a Design to an FPGA

C program   *Circuit*   *Array*

C = A+B

A → B → [+] → C

- CAD to translate circuit from text description to physical implementation well understood.

- CAD to translate from C program to circuit not well understood.

- Very difficult for application designers to successfully write high-performance applications
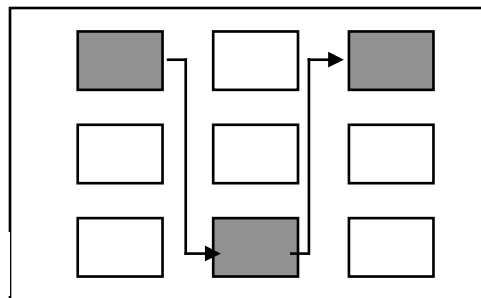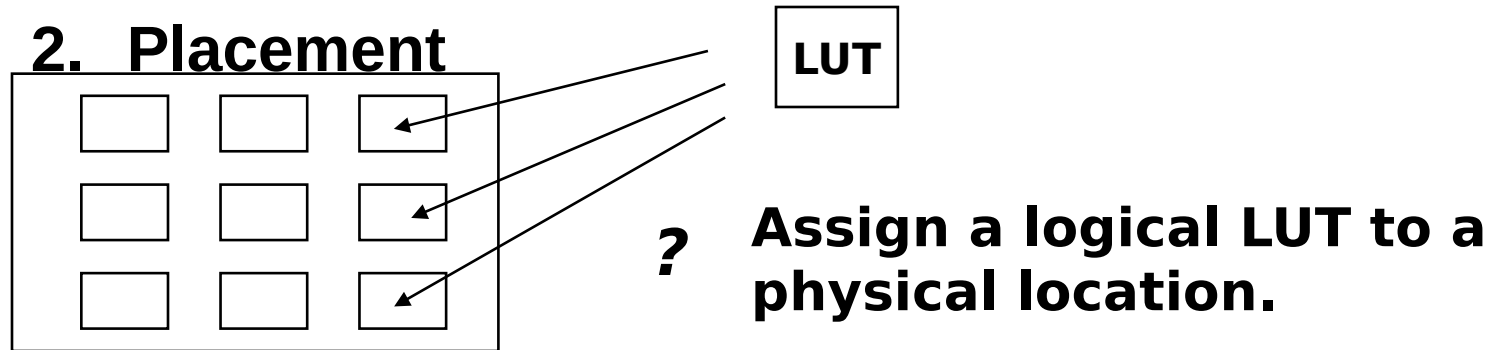
Need for design automation!

Circuit Compilation
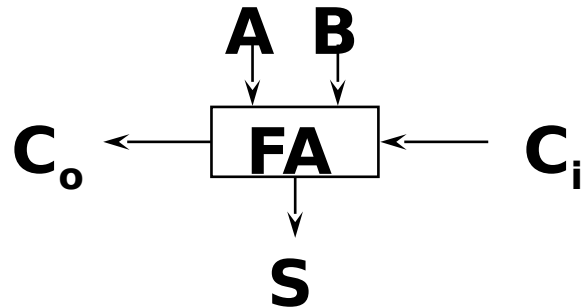
1. Technology Mapping

2. Placement

? **Assign a logical LUT to a physical location.**
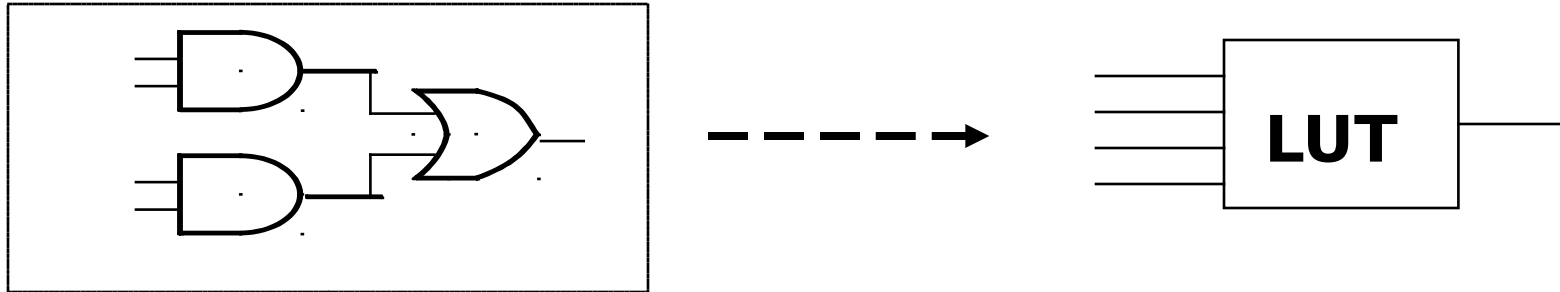
Select wire segments And switches for Interconnection.

Two Bit Adder

Made of Full Adders

A B

C_o ← **FA** ← C_i

S

$A+B = D$

Logic synthesis tool reduces circuit to SOP form

$S = ABC_i + A'B'C_i + AB'C_i' + A'BC_i'$

A
B
C_i → **LUT** — C_o

A
B
C_i → **LUT** — S
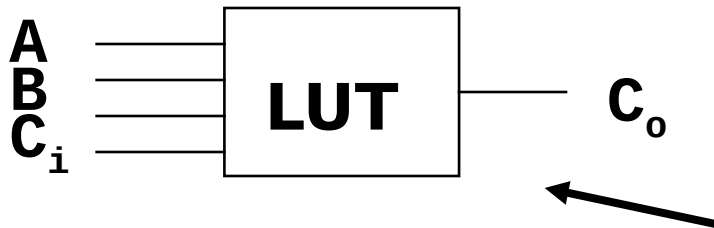
$C_o = ABC_i + A'BC_i + AB'C_i + ABC_i'$

Dynamic Reconfiguration
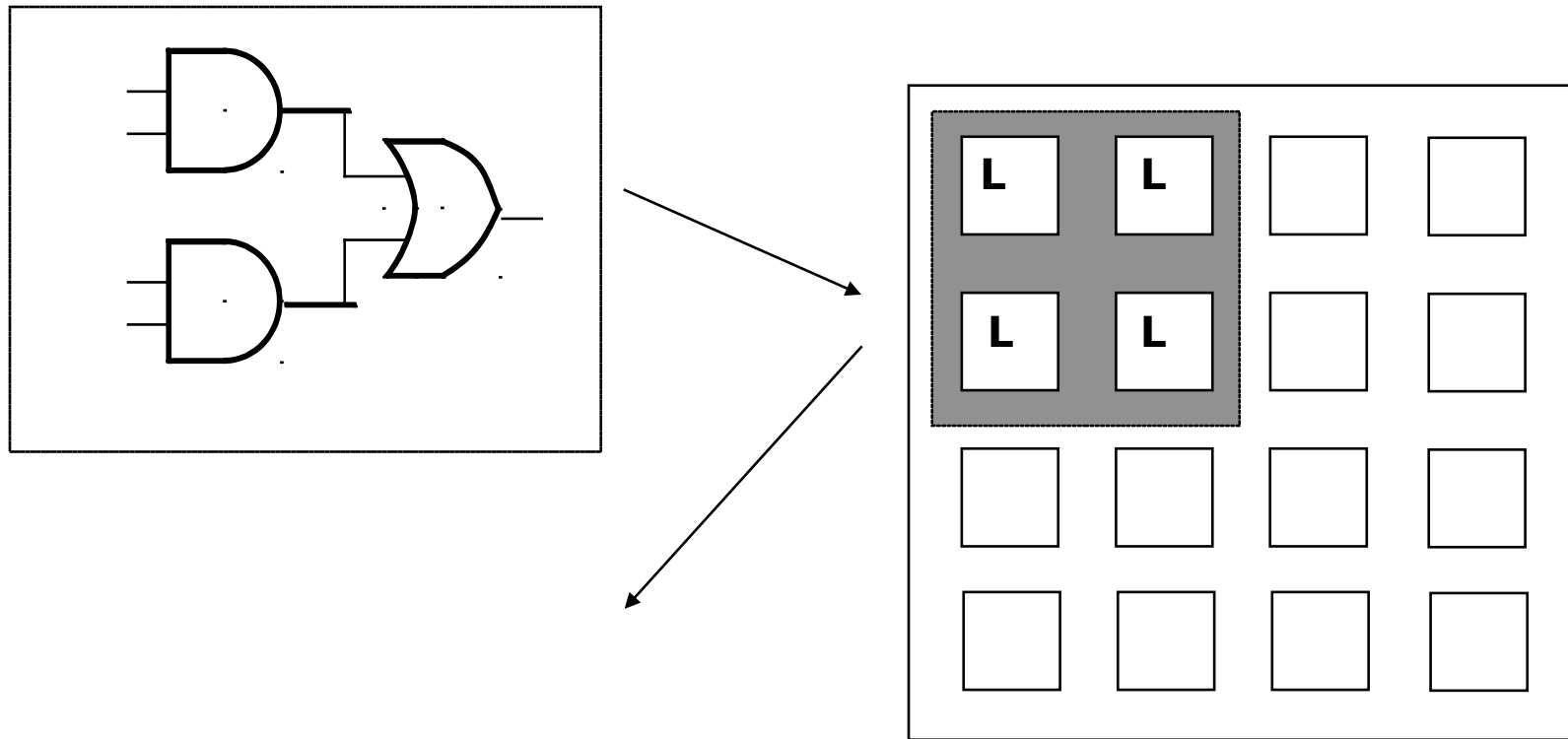
- **What if I want to exchange part of the design in the device with another piece?**

- **Need to create architectures and software to incrementally change designs.**

- **Effectively a "configuration cache"**
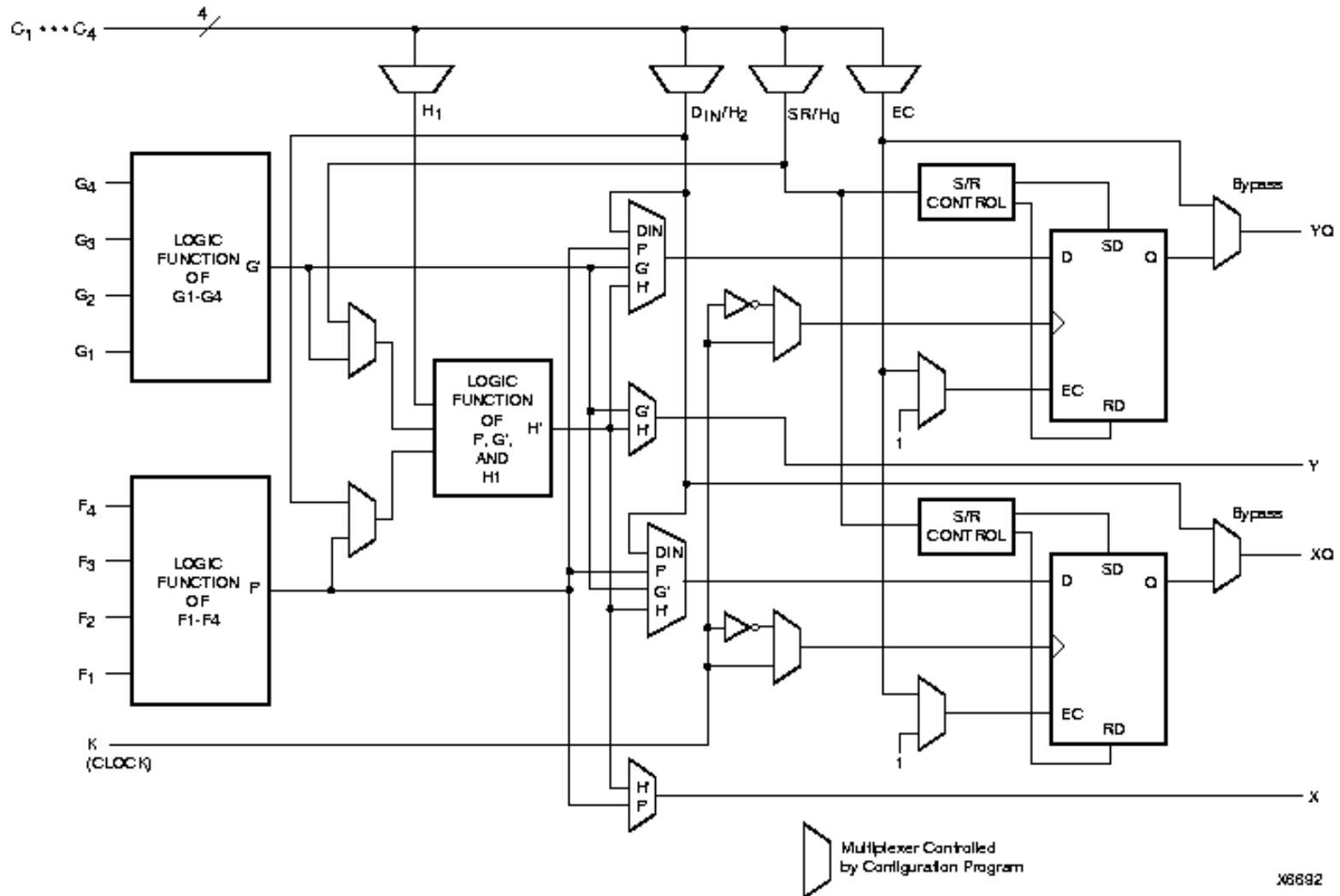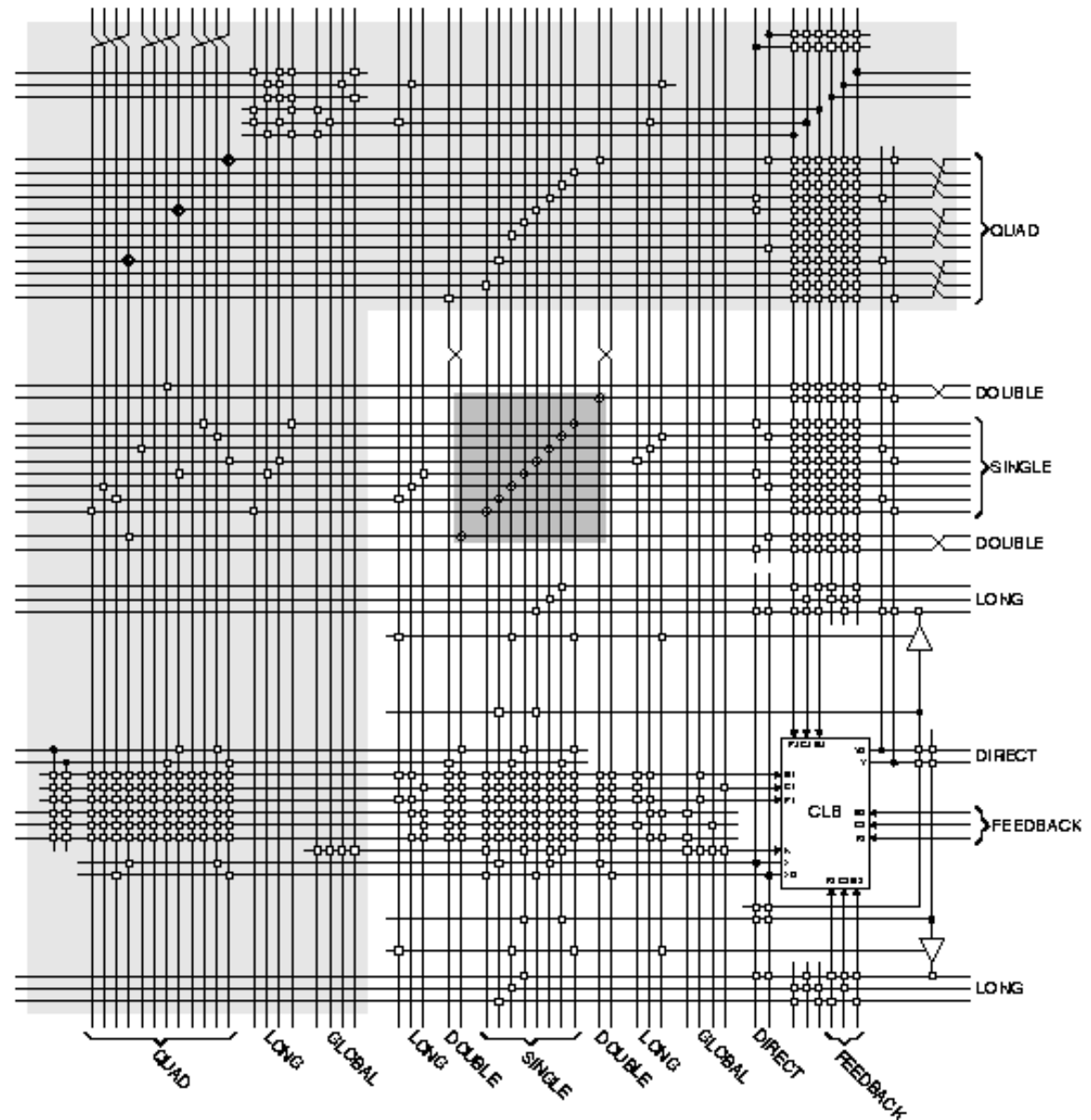
Xilinx XC4000 Cell

Figure 1: Simplified Block Diagram of XC4000 Series CLB (RAM and Carry Logic functions not shown)

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Xilinx XC4000 Routing

Small boxes represent switches

Summary

° **Programmable logic allows for designers to easily create custom designs**

° **Programmable array logic contains AND-OR structures to implement SOP equations**

° **FPGAs contain small memories and numerous wires for routing**

° **Designers create designs in Verilog**

  • **Design translated to the chip via software**

° **Hands on experience in ECE353, ECE354**